Available online at www.sciencedirect.com
SCIENCE DIRECT®
Sensors and Actuators A 114 (2004) 362–370
SENSORS AND ACTUATORS A PHYSICAL
www.elsevier.com/locate/sna

Micromachined CMOS thermoelectric generators as on-chip power supply

M. Strasser [a,*], R. Aigner [b], C. Lauterbach [c], T.F. Sturm [c], M. Franosch [b], G. Wachutka [d]

[a] *Infineon Technologies AG, Memory Products, 81541 Munich, Germany*
[b] *Infineon Technologies AG, Secure Mobile Solutions, 81730 Munich, Germany*
[c] *Infineon Technologies AG, Corporate Research, 81730 Munich, Germany*
[d] *Munich University of Technology, Institute for Physics of Electrotechnology, 80290 Munich, Germany*

Received 24 July 2003; received in revised form 18 November 2003; accepted 28 November 2003

Available online 25 January 2004

Abstract

As the power consumption of a large number of microelectronic devices has been continuously reduced in recent years, power supply units of a few microwatts have become sufficient for their operation. Our improved micro-scale thermoelectric generator (μ-TEG) is based on polysilicon surface micromachining and is designed to convert waste heat into electrical power. Since this device is compatible with standard CMOS fabrication processes, it can be easily integrated on chip level and matches the needs for low-cost and small-size systems. As thermoelectric materials, both, pure poly-Si and poly-$Si_{70\%}Ge_{30\%}$ have been investigated. Emphasis was placed on a thermally optimized design and the reduction of the total electrical resistance of the generator. As a result of these improvements, a voltage of 5 V and an electrical power output of 1 μW for a matched consumer is achieved with generators of 1 cm^2 in size at a temperature drop of about 5 K.

Keywords: Power supply; Surface micromachining; Thermal converter; Thermoelectric devices

1. Introduction

In many respects, thermoelectric generators (TEGs) show advantages compared to batteries: they are robust, consist of environmentally friendly materials and possess a virtually unlimited lifetime. However, for many years TEGs have been restricted to niche applications such as power supplies for space missions [1]. With increasing efficiency of the thermoelectric materials [2], decreasing power consumption of microelectronic circuitry and reduced production cost, thermoelectric devices may eventually be heading for important breakthroughs. Today, although expensive, the first wrist-watches powered by body-heat that are working on the thermoelectric principle are commercially available. The energy consumption of such a watch is specified to 1 μW with a driving voltage of 1.5 V [3]. Some other environments like those encountered in the automotive field or the domestic area provide higher temperature gradients and, therefore, promise a multitude of further applications. There is a significant difference between conventional, large-size thermoelectric generators and those on micro-scale: since a silicon-based chip is usually only some hundred micrometers thin, its internal thermal resistance is small compared to the thermal contacts of the surrounding assembly. This fact limits the thermal efficiency. Thus, there is a great challenge in increasing the generator's thermal resistance by means of micromachining and material optimization [4,5]. However, the advantage of a CMOS compatible silicon-based thermoelectric generator is obvious: the possibility of a monolithic on-chip integration including the microelectronic circuitry it is designed to power.

2. Theory

Due to the thermoelectric Seebeck effect, a temperature difference between both ends of a bar made of conducting or semiconducting material leads to a voltage generated over the bar. A thermocouple is made of two dissimilar thermoelectric bars joined at one end. Thermoelectric generators are composed of a large number of thermocouples which are electrically connected in series and that are arranged

* Corresponding author. Tel.: +49-89-234-57409; fax: +49-89-234-21258.
E-mail address: marc.strasser@infineon.com (M. Strasser).

0924-4247/$ – see front matter © 2004 Elsevier B.V. All rights reserved.
doi:10.1016/j.sna.2003.11.039

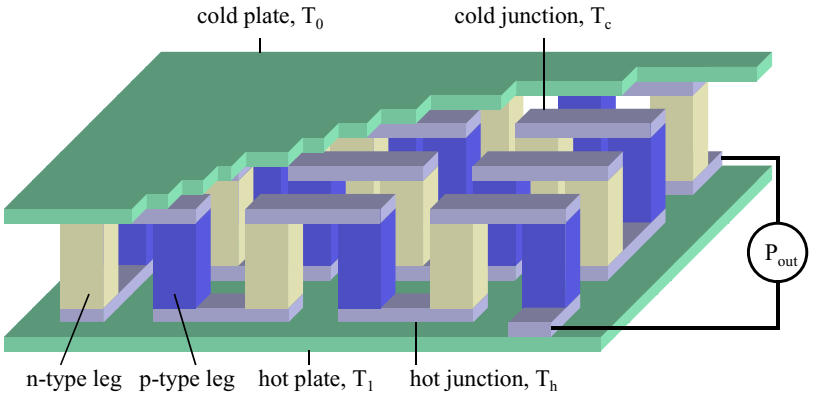

Fig. 1. Schematic view of a thermoelectric generator that consists of n- and p-type thermoelectric legs which are electrically connected in series and that are thermally arranged in parallel.

in meanders to make best use of a given area (see Fig. 1). Efficient thermoelectric generators should be built up of thermoelectric materials possessing a large Seebeck coefficient α, a low electrical resistivity ρ and a low thermal conductivity λ [6]. Large Seebeck effects are found in semiconducting materials which makes silicon an interesting choice for thermoelectric devices. Even more promising are compound semiconductors such as bismuth tellurides because of their low thermal conductivity [2]. However, these V–VI-semiconductors are difficult to produce and high efforts are necessary be made to make these materials compatible with standard silicon chip fabrication processes [7].

In sum, for a given relative Seebeck coefficient α of the two thermoelectric materials employed, the generated open-circuit voltage U_0 of a generator can be expressed by the number of thermocouples m and the temperature difference ΔT_g between the hot and the cold junctions:

$$U_0 = m\alpha\,\Delta T_g \tag{1}$$

Compared to the enclosing thermal resistors such as thermal contacts or heat sinks mounted to it, a μ-TEG possesses a rather small internal thermal resistance. As these additional thermal resistors will therefore affect the heat flow through the device, the system is not operated at a fixed temperature difference but rather under constant heat flow conditions. In this case, the output power instead of the thermal efficiency needs to be optimized [8]. Hence, as the system shall be operated at maximum electrical power output P_{out}, we have to match the electrical impedances in such a way that the Ohmic resistance of the generator is equal to the electrical resistance of the load:

$$P_{out} = U_{out} I = \frac{U_0^2}{4R_g} = \frac{m^2\alpha^2}{4R_g}(\Delta T_g)^2 \tag{2}$$

where $U_{out} = U_0 - IR_g$ is the output voltage under load, $I = U_0/2R_g$ is the electrical current in the matched case and R_g is the electrical resistance of the generator.

In order to derive an expression for the maximum power output just depending on the device materials and design parameters, ΔT_g has to be determined. For this purpose, the thermoelectric network of the generator has to be analyzed in analogy to an electric circuit. Here, the additional thermal resistors on the hot and cold side of the actual generator, the Peltier effect and Joule heating are taken into account. Thus, the total temperature drop ΔT rather than ΔT_g will be assumed to be given. If the generator is sandwiched between resistors with thermal resistances K_c and K_h at the cold and hot side, respectively, the individual temperature drops have to be added and can be expressed in terms of the corresponding heat currents q_c and q_h:

$$\Delta T = \Delta T_g + K_c q_c + K_h q_h \tag{3}$$

The energy balances for the cold and hot side must include the heat contributions by the Peltier effect and the Joule heating in the generator. This gives expressions for the heat flow q_h entering the hot junction and the heat flow q_c leaving the cold junction [4]:

$$q_h = \frac{2R_g}{2R_g + m^2\alpha^2 K_h\,\Delta T_g}\left(\frac{\Delta T_g}{K_g} + \frac{m^2\alpha^2 T_1\,\Delta T_g}{2R_g} - \frac{P_{out}}{2}\right), \tag{4}$$

$$q_c = \frac{2R_g}{2R_g - m^2\alpha^2 K_c\,\Delta T_g}\left(\frac{\Delta T_g}{K_g} + \frac{m^2\alpha^2 T_0\,\Delta T_g}{2R_g} + \frac{P_{out}}{2}\right) \tag{5}$$

where T_0 and T_1 are the temperatures at the cold and hot side of the entire device, respectively, and K_g is the inner thermal resistance of the generator. Inserting Eqs. (4) and (5) in Eq. (3) leads to a cubic equation in ΔT_g:

$$\Delta T = \Delta T_g\left[1 + \frac{1}{4K_g}\left(\frac{8K_cR_g + m^2\alpha^2K_cK_g\,\Delta T_g + 4m^2\alpha^2K_cK_gT_0}{2R_g - m^2\alpha^2K_c\,\Delta T_g} + \frac{8K_hR_g - m^2\alpha^2K_hK_g\,\Delta T_g + 4m^2\alpha^2K_hK_gT_1}{2R_g + m^2\alpha^2K_h\,\Delta T_g}\right)\right]. \tag{6}$$

This equation possesses three real solutions for physically valid parameters. As two of these solutions imply negative temperature values for T_c, only the third solution is of physical significance:

$$\Delta T_g = \frac{R_g}{m^2\alpha^2}\left[\frac{1}{K_c} - \frac{1}{K_h} + 2\,S\cos\left(\frac{1}{3}\arccos\left(\frac{r}{S^3}\right) + \frac{4\pi}{3}\right)\right], \quad (7)$$

where

$$r = \left(\frac{1}{K_c} - \frac{1}{K_h}\right) \times \left(\frac{1}{K_c^2} + \frac{2}{K_c K_h} + \frac{1}{K_h^2} + \frac{4}{K_g K_h} + \frac{4}{K_g K_c}\right) + 2\frac{m^2\alpha^2}{R_g}\left(\frac{T_0}{K_c^2} - \frac{T_1 - T_0}{K_c K_h} - \frac{T_1}{K_h^2}\right) \quad \text{and}$$

$$S = \sqrt{\frac{1}{K_c^2} + \frac{2}{3K_c K_h} + \frac{1}{K_h^2} + \frac{8}{3K_g}\left(\frac{1}{K_c} + \frac{1}{K_h}\right) + \frac{4}{3}\frac{m^2\alpha^2}{R_g}\left(\frac{T_0}{K_c} + \frac{T_1}{K_h}\right)}.$$

If this solution for ΔT_g is inserted into Eq. (2), an expression for the maximum electrical power output of the generator is obtained which depends on the external temperatures T_0 and T_1, the material properties and geometry only. This result reveals that a micro-scale thermoelectric generator (μ-TEG) operates in another regime than conventional large-scale TEGs (see Fig. 2).

From a material point of view, it is the Seebeck coefficient α, the electrical resistivity ρ and the thermal conductivity λ of the thermocouples that determine the power output of a μ-TEG. This can be observed in Eq. (7) considering that ρ enters the electrical resistance of the generator R_g and λ affects the thermal resistance of the generator K_g. Thus, it is important to get to know these material data in order to optimize the thermoelectric generator.

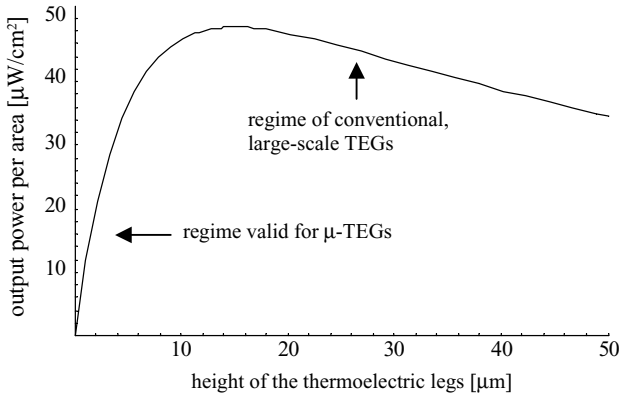

Fig. 2. Example of an ideal TEG with enclosing thermal resistors for $\Delta T = 5$ K: calculated output power per area as a function of the height of the thermoelectric legs. μ-TEGs are operated in the regime shown to the left.

3. Material properties

Although polysilicon layers of different thickness and doping concentration have been studied (see Figs. 3 and 4), only the results for 400 nm thick highly boron or phoshorous doped poly-Si and poly-$Si_{70\%}Ge_{30\%}$ layers will be discussed in detail. This is because just the highest doping concentration of $2.5 \times 10^{20}\,cm^{-3}$ provides a low total electrical resistance of the thermoelectric generator with regard to the consumer resistor that has to be matched. The Seebeck coefficient α the electrical resistivity ρ, the thermal conductivity λ, and the electrical contact resistance have been measured (see Table 1). The Seebeck coefficients have been extracted using special planar test structures [9]. The values of the electrical resistivity have been determined from van-der-Pauw Greek crosses [10]. The electrical contact

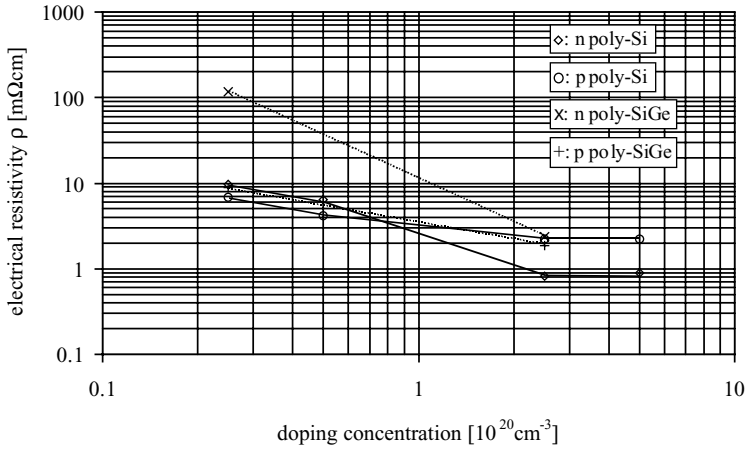

Fig. 3. Electrical resistivities of boron and phosphorous implanted pure polysilicon (solid lines) and poly-$Si_{70\%}Ge_{30\%}$ (dashed lines) vs. doping concentration determined at a temperature of 300 K.

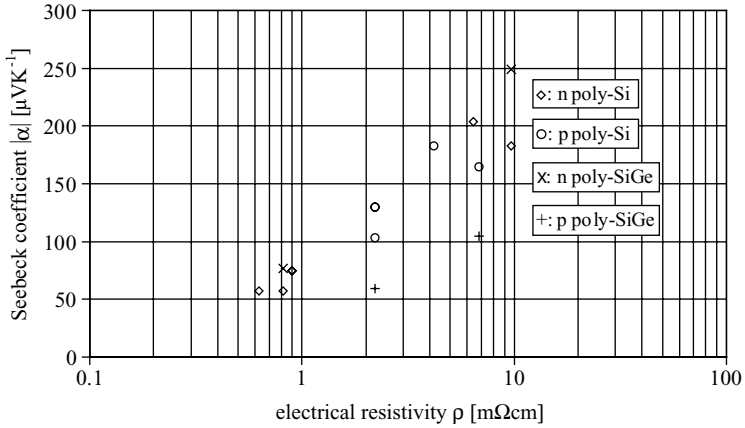

Fig. 4. Absolute value of the Seebeck coefficients of boron- and phosphorous-implanted pure polysilicon and poly-$Si_{70\%}Ge_{30\%}$ vs. the electrical resistivity of the material determined at a temperature of 300 K.

resistances could be derived via Kelvin structures [11]. The contacts between the polysilicon and the aluminum layer are made from tungsten to ensure a completely filled contact hole. For pure poly-Si the contact resistance with a tungsten stud sized to one square micrometer was found to be $R_{cn} = (4.0 \pm 0.1)\,\Omega$ for phosphorous implantation and $R_{cp} = (7.6 \pm 0.4)\,\Omega$ for boron doping. In the case of poly-$Si_{70\%}Ge_{30\%}$ values of $R_{cn} = (6.5 \pm 0.5)\,\Omega$ for phosphorous doping and $R_{cp} = (5.1 \pm 0.1)\,\Omega$ for boron implantation have been measured. Compared to our previous approach where no tungsten studs have been used [4], the contact resistances could be lowered significantly in this way.

A surface-micromachined structure was used to measure the thermal conductivities of the highly-doped polysilicon layers. For producing this thermal test structure, the polysilicon layer is patterned into two sets of beams and a heater connecting them (see Fig. 5). The 1.6 μm thick sacrificial oxide layer underneath the polysilicon is removed using HF etchant. Hence, a cavity is created below the actual device.

Applying an electrical current to the polysilicon heater, most of the generated heat current $q = UI$ is forced to flow into the beams perpendicular to it. However, the total heat flow q has to be reduced by the heat current q_{par} lost in the connectors of the heater yielding the remaining heat current q_b. A correction factor γ can be defined:

$$q_b = \gamma q = \gamma(q_b + q_{par}). \tag{8}$$

Solving Eq. (8) for γ and substituting q with $\Delta T/K$ enables to express γ by the thermal resistances K_{par} and K_b:

$$\gamma = \frac{K_{par}}{K_{par} + K_b}. \tag{9}$$

Thus, it is the parasitic thermal resistance K_{par} that needs to be determined. Let y be the coordinate directing parallel to the electrical current (see Fig. 6 for notation). Heat that is generated in a point of coordinate y_0 in the heater will be able to flow into both connectors of the heater. This means there are two thermal resistors in parallel for the y-direction. The length of these resistors are $s+y_0$ and $s+b-y_0$, respectively, where b is the total width of the beams and s is the length of a connector. For the total parasitic thermal resistance K_{par} all points y on the heater have to be integrated:

$$K_{par} = \frac{1}{b}\int_0^b \frac{1}{\lambda dg}\left(\frac{1}{s+y} + \frac{1}{s+b-y}\right)^{-1} \mathrm{d}y \tag{10}$$

where d is the layer thickness and g is the length of a connector of the polysilicon heater, yielding:

$$K_{par} = \frac{1}{6\lambda dg}\frac{b^2 + 6bs + 6s^2}{b + 2s}. \tag{11}$$

Table 1
Measured material properties for 400 nm thick poly-Si and poly-$Si_{70\%}Ge_{30\%}$ layers boron and phosphorous doped with a concentration of $2.5 \times 10^{20}\,cm^{-3}$

Material	Electrical contact resistance R_c (Ω)	Seebeck coefficient α ($\mu V K^{-1}$)	Electrical resistivity ρ (mΩ cm)	Thermal conductivity λ ($W m^{-1} K^{-1}$)
n-poly-Si	4.0 ± 0.1	−57 ± 9	0.813 ± 0.001	31.5 ± 3.7
p-poly-Si	7.6 ± 0.4	103 ± 17	2.214 ± 0.004	31.2 ± 3.7
n/p-poly-Si couples	5.8 ± 0.4	160 ± 19	1.514 ± 0.004	31.4 ± 5.2
n-poly-SiGe	6.5 ± 0.5	−77 ± 7	2.37 ± 0.04	9.4 ± 2.0
p-poly-SiGe	5.1 ± 0.1	59 ± 9	1.87 ± 0.01	11.1 ± 2.0
n/p-poly-SiGe couples	5.8 ± 0.5	136 ± 11	2.12 ± 0.04	10.3 ± 2.8

The highlighted values are calculated by averaging (ρ, λ and R_c) or addition (α) and hold for thermocouples.

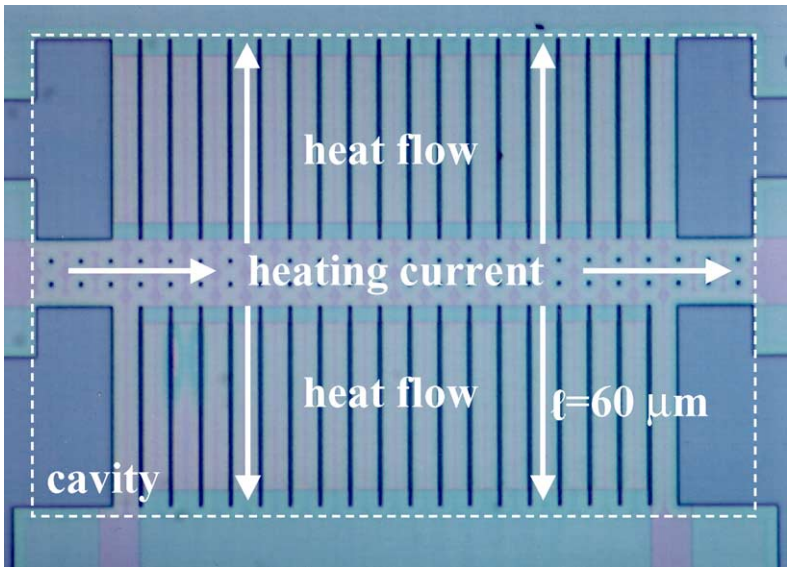

Fig. 5. Micrograph of a double-beam test structure to measure the thermal conductivity of polysilicon layers. The boundary of the cavity underneath the device is indicated by dashed lines.

With l denoting the length of a beam holds $K_b = \ell/(4\lambda db)$ [11] and γ becomes the purely geometrical expression:

$$\gamma = \frac{2b(b^2 + 6bs + 6s^2)}{2b^3 + 12b^2 s + 6g\ell s + 3bg\ell + 12bs^2}. \quad (12)$$

In that way, measuring under vacuum conditions, the thermal conductance of the beams and thus the thermal conductivity of the polysilicon itself can be deduced according to the relation [12]:

$$\lambda = \frac{\gamma UIR(T_0)\beta\ell}{4\,db\,\Delta R} \quad (13)$$

where $R(T_0)$ is the initial electrical resistance, β is the temperature coefficient of resistance, and $\Delta R = R(T_0)\beta\,\Delta T$ is the thermal change in Ohmic resistance.

The advantage of this surface micromachined thermal structure compared to previously presented ones [13] is not only the fact that it does not require any bulk micromachining but the novelty that the polysilicon layer is no sandwich with other materials such as SiO_2. Using this structure, the thermal conductivities of poly-Si and poly-$Si_{70\%}Ge_{30\%}$ have been measured (see Table 1). As expected [14,15], poly-$Si_{70\%}Ge_{30\%}$ shows a lower thermal conductivity compared to pure poly-Si [13].

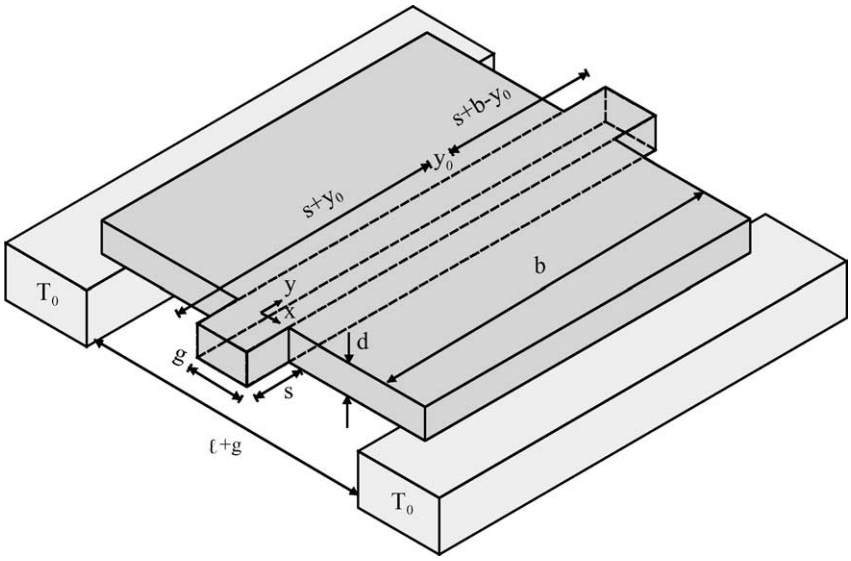

Fig. 6. Bridge structure to determine the thermal conductivity of a thin layer (dark gray). The heat sinks are drawn in light gray, the integrated heater is shown by dashed lines.

The entire set of material data is used to compare thermoelectric generators based on pure poly-Si to those made of poly-$Si_{70\%}Ge_{30\%}$ through coupled thermoelectric simulations.

4. Coupled thermoelectric simulations

Given the material properties, coupled thermoelectric simulations of possible generator designs have been performed prior to the realization. For this reason, half of a single generator cell was built as finite element model. On the silicon substrate, the basic thermal barrier between the cold and the hot side of the thermoelectric legs is realized by means of a field oxide layer (FOX). Underneath this barrier, there is an air filled cavity for additional thermal isolation. The thermoelectric leg is either consisting of pure poly-Si or poly-$Si_{70\%}Ge_{30\%}$. Its lower end is separated from the silicon substrate by a thin oxide layer. The upper end of the leg is situated on the field oxide barrier. Tungsten plugs and aluminum bridges are used to connect the thermoelectric legs to each other. A second metal bridge is added to the upper junction to improve the thermal coupling to the surface of the device. The polysilicon and the metalization are entirely encapsulated in oxide. A fixed temperature difference of 3 K between the bottom and the top of the generator cell is assumed as boundary condition for the thermal simulation using the FEM-tool ANSYS. The simulated temperature distribution of the optimized thermoelectric cell for the mentioned boundary conditions is shown in Fig. 7. After the first run, the junction temperatures and hence the temperature difference between the two ends of a thermoelectric leg are obtained. As this temperature difference causes two additional heat currents according to Eqs. (2), (4) and (5), further iterations of the simulation have to be performed including the heat generation at the junctions as boundary condition. After a few runs, the temperature difference between the two ends of a thermoelectric leg converges to a final value which determines the output power given by Eq. (2). The optimum parameters of the generator cell models have been determined by varying the length, the width and the thickness of the thermoelectric legs. The variable to be maximized in this analysis is the output power per area. In order to compare the power output of different thermoelectric generators, it is convenient to introduce a figure φ defined as the thermoelectric power generation per chip area A_g and per given temperature difference ΔT to the square:

$$\varphi = \frac{P_0}{A_g(\Delta T)^2}. \tag{14}$$

For both materials, poly-Si and poly-$Si_{70\%}Ge_{30\%}$, an optimum is found for legs of 6 μm width and 18.5 μm effective length at a layer thickness of 400 nm. With these dimensions, a single generator cell has an area of 49 μm × 10.9 μm. On a total area of 3.2 mm × 2.2 mm, 15,872 cells can be arranged in this way. Comparing pure poly-Si and poly-$Si_{70\%}Ge_{30\%}$, the coupled thermoelectric simulations show that the pure poly-Si type outperforms the poly-$Si_{70\%}Ge_{30\%}$ one with regard to the figure φ of thermoelectric power generation by 38%.

5. Experimental

The generator chips have been fabricated at an Infineon Technologies CMOS production facility. The basic thermal isolation between the cold and the hot side of the thermoelectric legs is achieved by means of a 1.6 μm thick thermal field oxide barrier (FOX). Both, samples with pure polysilicon as well as others containing poly-$Si_{70\%}Ge_{30\%}$ as

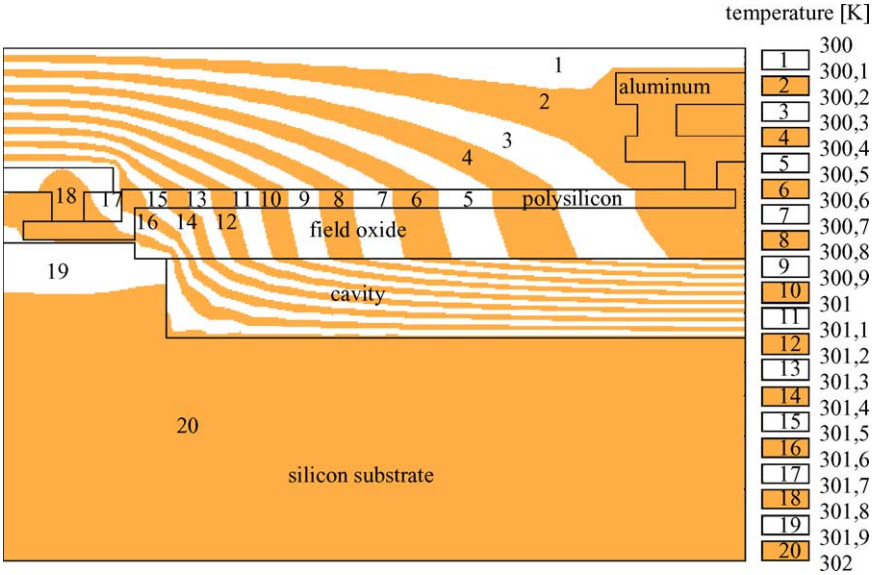

Fig. 7. FEM-simulated temperature distribution of the left half of a thermoelectric cell for a temperature drop of 3 K between bottom an top of the chip.

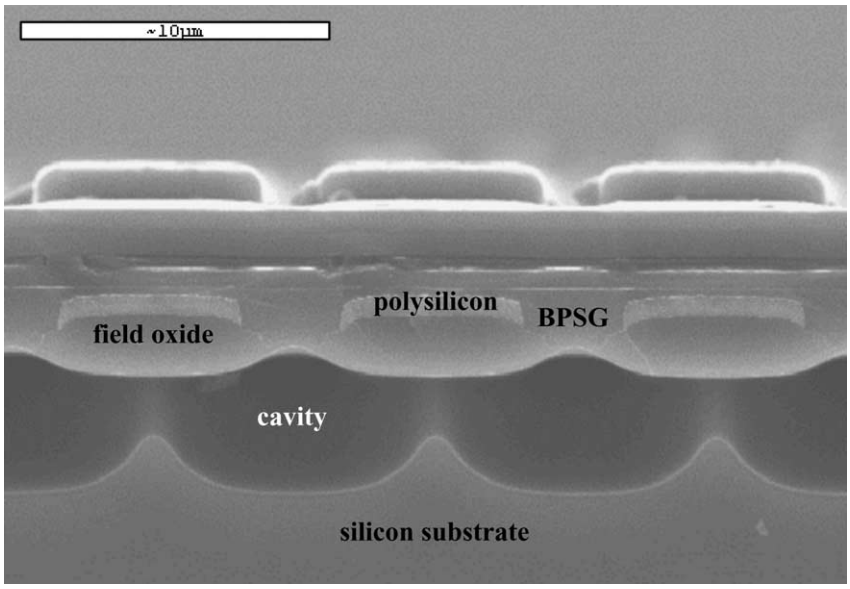

Fig. 8. SEM-micrograph showing the micromachined substrate cavity underneath the upper thermocouple junctions of a generator (view perpendicular to Figs. 7 and 9).

thermoelectric layer have been produced by chemical vapor deposition (CVD). The 400 nm thick thermoelectric layer is partially phosphorous-implanted with an energy of 130 keV to generate the n-legs and partially boron-implanted using 40 keV in other regions to form the p-legs, both employing a doping dose of $10^{16}\,cm^{-2}$. Afterwards, the polysilicon or poly-$Si_{70\%}Ge_{30\%}$ layer is patterned to release the thermoelectric legs. In order to optimize the heat flux direction within the generator, a micromachining etch step now is performed. During micromachining, the polysilicon legs are protected by an additional oxide mask perforated with holes to define the regions to be etched. Then, cavities are etched into the silicon substrate using isotropic CF_4 dry etching (see Fig. 8). The etch holes are closed with BPSG during the following oxide deposition step. Tungsten plugs and aluminum bridges are used to connect adjacent thermoelectric legs. A second metal bridge is added to every other junction to improve the thermal coupling to the surface of the device. The chip surface is passivated using a nitride and an oxide layer. An SEM-micrograph in Fig. 9 shows half of a thermoelectric cell with one polysilicon-leg.

The devices are tested in both ways, on wafer-level and as single chips. For the wafer-level measurement, an entire wafer is placed on a heatable thermochuck and a Peltier cooler is mounted on top. In this setup, the chips are connected electrically to a multimeter via tungsten probes. For the single-chip-measurement, the chips are sawn and wedge-bonded. Both measurement techniques give the same

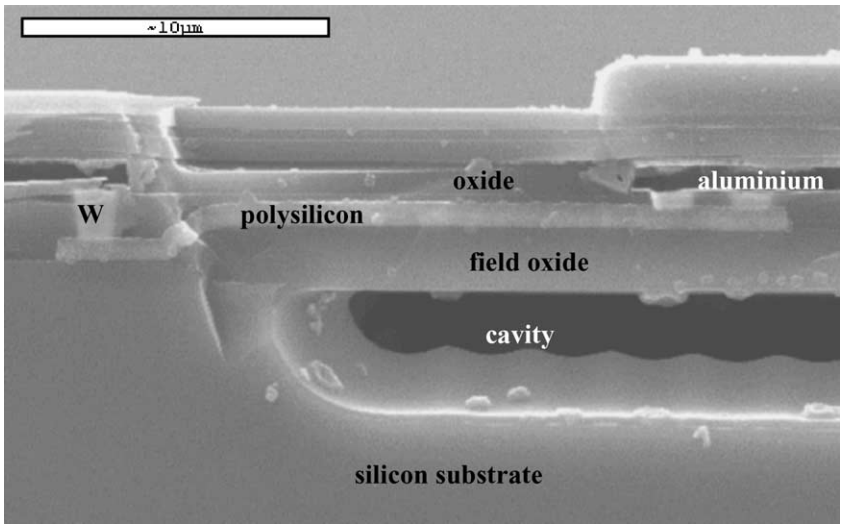

Fig. 9. SEM-micrograph showing the left half of a micromachined CMOS thermoelectric generator cell. The aluminum metallization was removed during sample preparation.

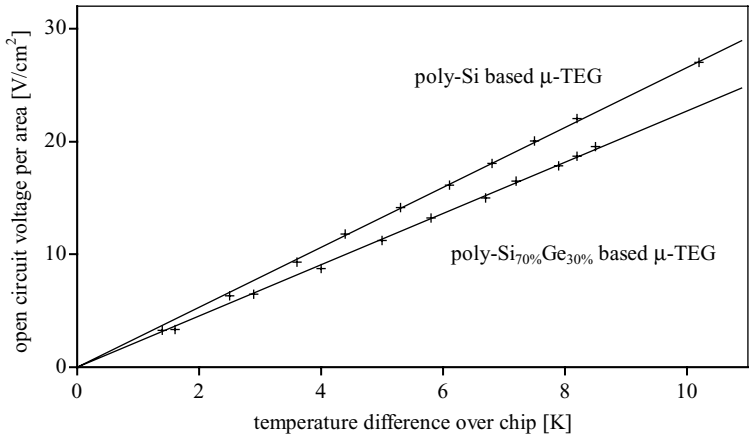

Fig. 10. Measured open circuit voltages per area of a μ-TEG based on pure polysilicon and another one based on poly-$Si_{70\%}Ge_{30\%}$ vs. the temperature drop between bottom and top of the chip.

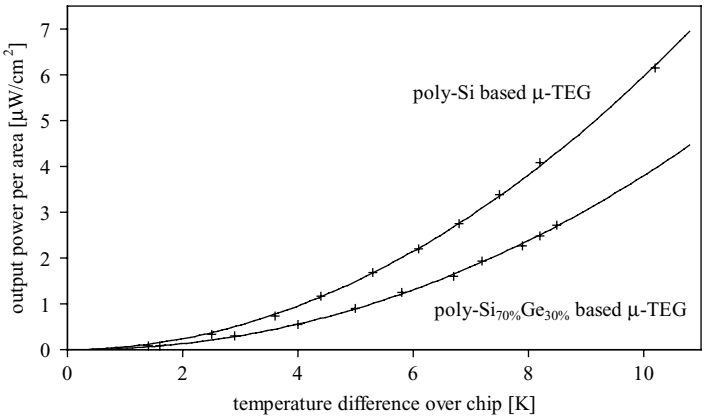

Fig. 11. Measured output power per area of a μ-TEG based on pure polysilicon and another one based on poly-$Si_{70\%}Ge_{30\%}$ vs. the temperature drop between bottom and top of the chip.

results. The open circuit voltage per area and per measured temperature difference for both, generators based on pure poly-Si and those using poly-$Si_{70\%}Ge_{30\%}$ is 2.2 V cm^{-2} K^{-1}. The determined output voltages per area for selected thermoelectric generators are shown in Fig. 10. In agreement with the predictions of the thermal simulations as discussed above, generators based on pure poly-Si outperform the devices employing poly-$Si_{70\%}Ge_{30\%}$ with respect to the power output per area. The figure of thermoelectric power generation φ is 0.0426 μW cm^{-2} K^{-2} for the μ-TEGs employing pure poly-Si and 0.0352 μW cm^{-2} K^{-2} for the ones based on poly-$Si_{70\%}Ge_{30\%}$. A graph of the output power per area versus the temperature difference for both generator types is displayed in Fig. 11. The total Ohmic generator resistance is 2.1 MΩ in the case of pure poly-Si and 2.5 MΩ for poly-$Si_{70\%}Ge_{30\%}$.

6. Discussion

In order to understand the particularities of micro-scale thermoelectric generators, the thermoelectric behavior of such devices has been investigated. One finding is that the output power of μ-TEGs strongly depends on the heat flux given by the environment. For optimum performance, as much as possible of the given heat has to be converted into electrical energy. For pure poly-Si and poly- $Si_{70\%}Ge_{30\%}$, the relevant material properties have been extracted using specially designed microstructures. Coupled thermoelectric simulations revealed that for maximum output power, pure poly-Si should be used to build up the micromachined CMOS generators. This result was verified in experimental tests. The different types of generators have been fabricated and tested successfully. If the presented poly-Si thermoelectric generator is sized to 1 cm^2, a temperature drop of about 5 K results in a voltage of more than 5 V and an electrical power output of about 1 μW for a matched consumer load. This is sufficient to power an electronic wrist watch by body heat.

References

[1] C.B. Vining, Semiconductors are cool, Nature 413 (2001).

[2] R. Venkatasubramanian, Thin-film thermoelectric devices with high room-temperature figures of merit, Nature 413 (2001).
[3] M. Kishi, H. Nemoto, T. Hamao, M. Yamamoto, S. Sudou, M. Mandai, S. Yamamoto, Micro-Thermoelectric Modules and Their Application to Wrist-watches as an Energy Source, in: Proceedings of IEEE 18th International Conference on Thermoelectrics, 1999, pp. 301–307.
[4] M. Strasser, R. Aigner, M. Franosch, G. Wachutka, Miniaturized thermoelectric generators based on poly-Si and poly-SiGe surface micromachining, Sens. Actuators A 97–98 (2002) 528–535.
[5] H. Glosch, M. Ashauer, U. Pfeiffer, W. Lang, A thermoelectric converter for energy supply, Sens. Actuators A 74 (1999) 246–250.
[6] R.R. Heikes, R.W. Ure, Thermoelectricity: Science and Engineering, Interscience Publishers, 1961.
[7] H. Boettner, A. Schubert, K.H. Schlereth, D. Eberhard, A. Garikov, M. Jaegle, G. Kuehner, C. Kuenzel, J. Nurnus, G. Plescher, New thermoelectric components using micro-system-technologies, in: Proceedings of the Sixth European Workshop on Thermoelectrics, Freiburg, Germany, 20–21 September 2001.
[8] G. Min, D.M. Rowe, in: D.M. Rowe (Ed.), Peltier Devices as Generators, CRC Handbook of Thermoelectrics, CRC Press, 1995.
[9] M. Strasser, R. Aigner, G. Wachutka, Analysis of a CMOS low power thermoelectric generator, Proc. Eurosens. XIV (2000) 17–20.
[10] M.I. Newsam, A.J. Walton, M. Fallon, Numerical analysis of the effect of geometry on the performance of the Greek cross structure, in Proceedings of the IEEE International Conference on Microelectronic Test Structures'96, 1996, pp. 247–252.
[11] S.J. Proctor, L.W. Lindholm, J.A. Mazer, Direct measurements of interfacial contact resistance, end contact resistance, and interfacial contact layer uniformity, IEEE Trans. Electron Devices 30 (11) (1983) 1535–1542.
[12] F. Völklein, Characterization of the Thermal Properties of Bulk and Thin-Film Materials by Using Diagnostic Microstructures, Micrometrology Symposium, Delft, The Netherlands, 31 August to 1 September 2000, pp. 91–107.
[13] M. von Arx, O. Paul, H. Baltes, Process-dependent thin-film thermal conductivities for thermal CMOS MEMS, J. Microelectromech. Syst. 9 (1) (2000) 136–145.
[14] C.B. Vining, in: D.M. Rowe (Ed.), Silicon Germanium, CRC Handbook of Thermoelectrics, CRC Press, 1995.
[15] P. Van Gerwen, K. Baert, R. Mertens, Thin Film Poly-$Si_{70\%}Ge_{30\%}$ for Thermopiles, Micro System Technologies 98, Potsdam, Germany, 1–3 December 1998, pp. 655–658.

Biographies

Marc Strasser was born in Düsseldorf, Germany, in 1972 where he studied physics at Heinrich Heine University. In 1998, he finished his diploma degree at Siemens Semiconductors in Munich doing research in electromigration of CMOS metallizations. From 1998 to 2002 he was with Corporate Research and the MEMS group of Infineon Technologies AG, working towards his DSc degree at Munich University of Technology. In this time, he was focusing on the thermoelectric properties of CMOS materials and the development of integrated thermoelectric devices. Since 2002, he is with the Memory Division of Infineon doing process and device simulations for the development of the next DRAM generations.

Robert Aigner received his PhD degree from Munich University of Technology in 1996 for research on micromachined chemical sensors. He was a visiting scientist at Berkeley Sensors and Actuators Center BSAC in 1996 where he worked on system design for inertial sensors. After that he joined the research group for MEMS at Siemens Corporate Technology in 1997. Since 1999 he is responsible for MEMS research at Infineon Technologies. His activities have a focus on advanced automotive sensors and MEMS for communication technologies. As a representative for his company he is member of several European institutions and committees for microsystem technology and was recently nominated as MEMS-expert for European Commission's research projects.

Christl Lauterbach was born 1959 in Moenchroeden, Germany and graduated from Siemens School, Munich in communication engineering. She joined the Corporate Research Laboratories of Siemens AG in Munich, Germany, working in the photonic group on technology and device development of infrared emitting diodes and fast photoreceivers. In 1995, she joined the microelectronics IC group, where she was engaged in CMOS basic circuit design, adiabatic circuits, as well as the development of fuse and antifuse structures. Since 1999 Christl Lauterbach has been with Corporate Research of Infineon Technologies, Munich. She is working as senior staff engineer on emerging technologies, including wearable electronics and smart textiles. Her main interest in wearable electronics are microelectronic/textile interconnect and energy conversion in clothes. She has authored or coauthored some 50 scientific papers.

Thomas Sturm was born in Landshut, Bavaria, in 1966 and studied mathematics and computer sciences at the Munich University of Technology (MUT) where he gained his diploma degree in 1990. Afterwards, he was a scientific assistant at the MUT working in the field of nonlinear optimization theory and he was granted a doctorate in mathematic in 1992. He joined Siemens Public Communication Networks in 1995 as software developer for pre-product evaluations. From 1997 on, he worked as project scientist at Siemens Corporate Technology with mathematical optimization, stochastic algorithms and decoding methods for communications as main research fields. Since 2001, he is with Infineon Corporate Research with responsibility for numerical algorithms and system architectures for ambient intelligence projects.

Martin Franosch received his diploma in physics at Munich University of Technology (in collaboration with GSI, Darmstadt) for research in nuclear physics in 1985. Until 1985 he continued this work as scientific assistant at Munich University of Technology. In 1986 he joined the new e-beam group at the Siemens Corporate Research and Development Department. From 1990 to 1992 he was doing research on phase shift masks. Since 1992 he is working in process development of silicon-, silicon/germanium- and germanium-CVD processes for different bipolar and CMOS applications and micromechanical sensors. Since 1999 he is a member of the MEMS group at Infineon Technologies.

Gerhard K. M. Wachutka received the DSc degree from the Ludwig-Maximilians-Universität, Munich, Germany, in 1985. From 1985 to 1988, he was with Siemens Corporate Research & Development, Munich, where he headed a modeling group active in the development of modern high-power semiconductor devices. In 1989, he joined the Fritz-Haber-Institute of the Max-Planck-Society, Berlin, Germany, where he worked in the field of theoretical solid-state physics. From 1990 to 1994, he was head of the micro-transducers modeling and characterization group of the Physical Electronics Laboratory at the Swiss Federal Institute of Technology (ETH), Zurich. There, he also directed the micro-transducers modeling module of the Swiss Federal Priority Program M2S2 (Micromechanics on Silicon in Switzerland). Since spring 1994, he has been heading the Institute for Physics of Electrotechnology at the Munich University of Technology, where his research activities are focussed on the design, modeling, characterization, and diagnosis of the fabrication and operation of semiconductor microdevices and microsystems. He has authored or coauthored more than 180 publications in scientific or technical journals. He is consultant of research institutes in industry and university, and he serves as reviewer for various scientific journals and other institutions. Among his many educational activities, he has set up and taught courses funded by European Community training programmes such as UETP, EUROFORM, and EUROPRACTICE. Professor Wachutka is member of the IEEE, the American Electrochemical Society, the American Materials Research Society, the ESD Association, the German Physical Society, and the AMA Society for Sensorics.